|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| instruction | job | Opc(6) | R0(5) | R1(5) | R2(5)  addr(16) off(16) | Imm(32) | length |
| MTC | Move to float coprocessor | 100000 | - | - | - | - | 32 bits |
| MFC | Move from float coprocessor | 111111 | - | - | - | - | 32 bits |
| ADDF | DST ← SRC1 + SRC2 | 100001 | 5 | 5 | 5 | - | 32 bits |
| SUBF | DST ← SRC1 - SRC2 | 100010 | 5 | 5 | 5 | - | 32 bits |
| MULF | DST ← SRC1 \* SRC2 | 100011 | 5 | 5 | 5 | - | 32 bits |
| DIVF | DST ← SRC1 / SRC2 | 100100 | 5 | 5 | 5 | - | 32 bits |
| INVF | DST ← 1 / SRC | 100101 | 5 | 5 | - | - | 32 bits |
| ABSF | DST ← int32(SRC) | 100110 | 5 | 5 | - | - | 32 bits |
| COMF | SRC1 > SRC2 : DST = 1 , SRC1 < SRC2 : DST = -1 , SRC1 == SRC2 : DST = 0 | 100111 | 5 | 5 | 5 | - | 32 bits |
| MOVIF | DST ← IMM | 110000 | 5 | 5 | - | 32 | 64 bits |
| ADDIF | DST ← SRC + IMM | 110001 | 5 | 5 | - | 32 | 64 bits |
| SUBIF | DST ← SRC - IMM | 110010 | 5 | 5 | - | 32 | 64 bits |
| MULIF | DST ← SRC \* IMM | 110011 | 5 | 5 | - | 32 | 64 bits |
| DIVIF | DST ← SRC / IMM | 110100 | 5 | 5 | - | 32 | 64 bits |
| INVIF | DST ← 1 / IMM | 110101 | 5 | 5 | - | 32 | 64 bits |
| ABSIF | DST ← int32(IMM) | 110110 | 5 | 5 | - | 32 | 64 bits |
| LF = LW | VR ← MEM [$AR+ SIGN EXTEND (Offset)] | 111000 | 5 | 5 | 16 | - | 32 bits |
| SF = SW | MEM [$AR+ SIGN EXTEND (Offset)] ← VR | 111001 | 5 | 5 | 16 | - | 32 bits |
| BEQF | REG1 == REG2 : PC ← PC + SIGN EXTEND ( Address | “00” ) | 111100 | 5 | 5 | 16 | - | 32 bits |
| BLTF | REG1 < REG2 : PC ← PC + SIGN EXTEND ( Address | “00” ) | 111101 | 5 | 5 | 16 | - | 32 bits |
| BGTF | REG1 > REG2 : PC ← PC + SIGN EXTEND ( Address | “00” ) | 111110 | 5 | 5 | 16 | - | 32 bits |
| HLT | STOP PC | 000000 | - | - | - | - | 32 bits |